Patent Application No. 09/449,022
KLA-Tencor Corporation
METHOD AND APPARATUS FOR INSPECTING RETICLES IMPLEMENTING PARALLEL PROCESSING

Affidavit

I, Lawrence R. Miller, MD, PhD, declare as follows:

1. My education includes a PhD degree in physics from the University of California, Berlekey. I have worked in the area of semiconductor inspection for over 9 years. Specifically, I have worked on the design of inspection systems and I have designed electronic processing systems and associated firmware and software for photomask and wafer inspection systems. I am currently employed by KLA-Tencor, Corp. as Senior Principal Engineer.

2. I have analyzed the U.S. Patent 5,659,630 by Forslund (herein referred to as the Forslund patent), as well as the U.S. Patents 4,174,514 and 4,484,349 which are referenced in Forslund.

3. Forsland is clearly directed at only pipelined image processing systems, as opposed to patch processing systems. There is no mention of a system that puts an entire rectangle (patch) of pixels in a processor's local storage at a given time and then has the processor process the stored pixels when the processor is ready. There is no mention for example in Forsland of memory or buffering associated with a processor capable of storing a patch or rectangle of data.

Some of the above-mentioned patents mention storages that hold an entire image but these storages are just the overall input and output storages. They are not associated with particular processors in a multi-processor system.

4. Forslund only describes the use of pipelined image processing systems, rather than the use of patch processing systems. In Forslund, a set of adjacent rasterlines is delivered to one or more processors. For example all the pixels on a set of 16 raster lines are delivered, then the pixels on the next set of 16 lines is delivered. The example of using sets of 16 raster lines works in detail as follows. The 16 pixels which consist of the first pixel on each of the 16 raster lines

are delivered simultaneously to one or more processors, then the 16 pixels which consist of the second pixel on each of the raster lines are delivered simultaneously in the next time slot to these processors, then the 16 pixels which consist of the third pixel on each of the raster lines are delivered simultaneously in the next time slot to these processors, etc. What is clear is that Forslund describes a pipelined system, in which a processor processes the pixels currently being delivered to it and does not store the delivered pixels for more than a few (say 16) time slots. Thus the pixels are processed within a very short period of time after they are received. The scanning of pixels and the processing of the pixels occurs nearly synchronously. This is a major characteristic of a pipelined system. A patch processing system does not have this characteristic: in a patch-processing system, a storage associated with a given processor holds an entire rectangular area of pixels; the processor can therefore process the pixels asynchronously with respect to the pixel acquisition.

5. All of the examples described in Forslund implement a pipelined system. Specifically, the example of Figure 4B describes feeding half of the image to a first set of processors and half of the image to a second set of processors. However, it is clear from the cross referenced patents U.S. Patent No. 4,174,514 to Sternberg and No. 4,484,349 to McCubbrey that the image halves are still processed by a pipeline system.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

Lawrence R. Miller

Lawrence R. Miller, MD, PhD

7/19/2005

Date